REMARKS

Claims 1 - 15 are currently pending in this patent application.

Claims 1, 3, 5 and 12 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated December 4, 2002.

With respect to the Examiner's comments on the title of the invention, as indicated above, the applicants have amended the title of the invention, in its entirety, so as to read as follows: "SEMICONDUCTOR DEVICE WITH SURGE PROTECTIVE COMPONENT AND METHOD OF MANUFACTURING THE SEMICONDUCTOR DEVICE."

The applicants respectfully request that the title of the invention be approved by the Examiner, and that the outstanding objection to the title of the invention be withdrawn.

With respect to the Examiner's comments on the drawings, the applicants respectfully submit herewith a Request for Approval of Drawing Corrections, along with proposed drawing corrections to 5c, 5d and 6, as marked in red ink. More particularly, it is proposed that in Figures 5c, 5d and 6,

reference numbers "35a" and "35b" be changed to "25a" and "25b", respectively, and have such reference numbers 25a and 35b be directed to the first moat and the second moat, respectively.

The applicants respectfully request that the proposed drawing corrections be approved by the Examiner, and that the outstanding objections to the drawings be withdrawn.

As to the claims, the applicants thank the Examiner for now withdrawing the Webb patent (U.S. Patent No. 5,479,031), previously relied upon by the Examiner as a primary reference in the last Action.

However, the Examiner now relies on new references in rejecting the claims for reasons more fully discussed below.

With respect to the Examiner's comments on the language of claims 3 and 5, in the last full sentence on page 2 of the outstanding Action, the applicants respectfully submit herewith amendments to these claims, which address this matter.

Claim 1 stands rejected under 35 USC §112, second paragraph, for the specific reasons set forth in the third full paragraph on page 3 of the outstanding Action. The applicants respectfully request reconsideration of this rejection.

As indicated above, claims 1 has been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention, and in order to correct certain informalities therein, including those pointed out by the Examiner.

Accordingly, the withdrawal of the outstanding indefiniteness rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, the following rejections are set forth based on the Examiner's reliance on new references:

(1) claims 1 and 7 - 9 are rejected under 35 USC §102(b) as being anticipated by Takizawa (5,962,878);

(2) claim 2 is rejected under 35 USC 103(a) as being unpatentable over Takizawa (5,962,878) in view of Ohta (5,352,905);

(3) claims 3, 6, 10 and 12 - 14 are rejected under 35 USC §103(a) as being unpatentable over Takizawa (5,962,878) and Ohta (5,352,905), and further in view of Assour (4,292,646);

(4) claims 4, 11 and 15 are rejected under 35 USC §103(a) as being unpatentable over Takizawa (5,962,878), Ohta (5,352,905) and Assour (4,292,646), and further in view of Planey (3,772,577); and

(5) claim 5 is rejected under 35 USC §103(a) as being unpatentable over Takizawa (5,962,878), Ohta (5,352,905) and Assour et al. (4,292,646), and further in view of Casey (U.S. 6,448,589).

The applicants respectfully request reconsideration of these rejections.

Significant features of the applicants' claimed invention include the first and second emitter layers being at least partially embedded within the first and second base layers, respectively.

The primary reference of Takizawa is directed to a device having a semiconductor substrate 2, emitter-push restraining layers 16, emitter layers 18, base layers 20, and buried layers 46. In Takizawa, the emitter layer 18 is formed and extends along one side of the base layer 20.

On the other hand, in the applicants' semiconductor device:

> the first and second emitter layers 22a and 22b are formed on the insides of the first and second base layers 13a and 13b, respectively.[1]

With such structural arrangements:

> [t]he first and second emitter layers 22a and 22b are formed in the shape of a mesh. This means that the surfaces of the first and second base layers 13a and 13b are exposed in dotted state within the region where the surfaces of the first and second emitter layers 22a and 22b are positioned.[2]

It is the applicants' position that such structural arrangements are not disclosed by Takizawa's mere teachings of the emitter layer 18 being formed and extending along one side of the base layer 20.

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[1]See, lines 9-11, page 16 of the applicants' specification.

[2] See, the sentence bridging page 16 and 17 of the applicants' specification.

As to the secondary references, the Examiner's reliance thereon are limited and narrow. For example, Ohta is merely relied upon for teaching a first metal film T_1, and a second metal film T_2, while Assour is narrowly relied upon for teaching a ring-shaped moat 69. The secondary reference of Planey is narrowly relied upon for teachings moats 12 filled with oxide, while Casey's positioning of the base layers is relied upon.

However, the secondary references, singly or in combination, do not supplement the above-discussed deficiencies in the teachings of the primary reference of Takizawa in failing to fully meet the applicants' claimed invention; specifically, "the first and second emitter layers being at least partially embedded within the first and second base layers, respectively."

In view of the above, the applicants' respectfully submit that since not all of the applicants' claimed elements or features are found in exactly the same situation and united in the same way to perform the identical function in Takizawa's apparatus or in the manufacturing thereof, there can be no anticipation of the applicants' claimed invention, as now set forth in the claims, under 35 USC §102(b) based on Takizawa.

Accordingly, the withdrawal of the outstanding anticipation rejection under 35 USC §102(b) based on Takizawa (5,962,878) is in order, and is therefore respectfully solicited.

Moreover, the applicants respectfully submit that even if, *arguendo*, the teachings of the cited references can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicants' claimed invention. As such, a person of ordinary skill in the art would not have found the applicants' claimed invention obvious under 35 USC 103(a) based on Takizawa, singly or in combination with the secondary references.

Accordingly, the withdrawal of the outstanding obviousness rejections under 35 USC 103(a) based on Takizawa (5,962,878) in view of the cited secondary references is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

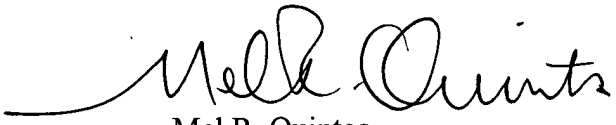
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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Enclosures: Version with markings to show changes made
Request for Approval of Drawing Corrections

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IN THE CLAIMS:

Amend claims 1, 3, 5 and 12 as follows:

1. (Twice Amended) A semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is provided as a second conductivity type, a semiconductor substrate of the first conductivity type, the semiconductor device comprising:

first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate;

first and second emitter layers of the first conductivity type;

first and second base layers of the second conductivity type, the first and second emitter layers being at least partially embedded within the first and second base layers, respectively;

and a substrate layer constituted by the semiconductor substrate,

wherein the substrate layer is sandwiched between the first and second buried layers,

wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN planar junctions with the first and second buried layers, said PN planar junctions extending along the first and second base layers and the first and second buried layers,

wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second base layers

wherein at least a part of the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and

wherein at least a part of the first and second buried layers are located between the first and second base layers and the substrate layer.

3. (Amended) The semiconductor device of claim 2, wherein ring-shaped first and second moats with bottom surfaces reaching the buried layers are formed on both sides of the semiconductor substrate, and wherein the first and second emitter layers are located on the inside of the first and second moats.

5. (Amended) The semiconductor device of claim 3, wherein at least a part of the first and second base layers are positioned at a region on the outside of the first and second moats of the surfaces of the semiconductor substrate.

12. (Amended) A semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is defined as a second conductivity type,

a semiconductor substrate of the first conductivity type, the semiconductor device comprising:

first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate;

first and second emitter layers of the first conductivity type;

first and second base layers of the second conductivity type, the first and second emitter layers being at least partially embedded within the first and second base layers, respectively;

a substrate layer constituted by the semiconductor substrate,

ring-shaped first moat is provided on the surface of the first base layer,

and ring-shaped second moat is provided on the surface of the second base layer,

wherein the substrate layer is sandwiched between the first and second buried layers,

wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN junctions with the first and second buried layers,

wherein the first and second emitter layers are located in a vicinity of a surface of inside of the first and second base layers so as to form PN junctions with the first and second base layers,

wherein at least a part of the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and

wherein at least a part of the first and second buried layers are located between the first and second base layers and the substrate layer,

wherein the first moat having bottom surfaces reaching the first buried layer, and both outer periphery and inner periphery of the first moat are in contact with the first base layer,

wherein the second moat having bottom surfaces reaching the second buried layer, and both outer periphery and inner periphery of the second moat are in contact with the second base layer.